





#### EB13C3 E 2 H -32.768M

Series —
RoHS Compliant (Pb-free) Low Current 3.3V 4 Pad
5mm x 7mm Ceramic SMD LVCMOS Oscillator

Frequency Tolerance/Stability – ±25ppm over 0°C to +70°C Nominal Frequency 32.768MHz

Logic Control / Additional Output Tri-State (High Impedance)

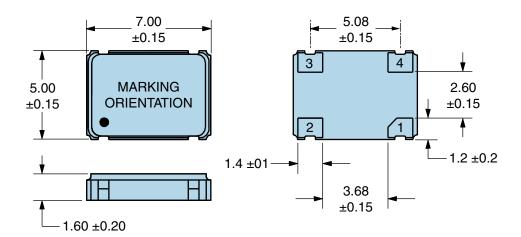
Duty Cycle -50 ±5(%)

Nominal Frequency         32.768MHz           Frequency Tolerance/Stability         ±25ppm over 0°C to +70°C (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Ouput Load Change, First Year Aging at 25°C, Shock, and Vibration)           Supply Voltage         3.3Vdc ±10%           Input Current         5mA Maximum           Output Voltage Logic High (Voh)         90% of Vdd Minimum           Input Current Logic High (Ioh)         1.6mA           Output Voltage Logic Low (Vol)         10% of Vdd Maximum           Input Current Logic Low (Iol)         +1.6mA           Rise/Fall Time         4nSec Maximum (Measured at 20% to 80% of waveform)           Load Drive Capability         50 ±5(%) (Measured at 50% of waveform)           Load Drive Capability         5mS           Logic Control / Additional Output         7ri-State (High Impedance)           Tri-State Input Voltage (Vih and Vil)         90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)           Standby Current         10µA Maximum (Disabled Output: High Impedance)           Start Up Time         10mSec Maximum           Storage Temperature Range         -55°C to +125°C	ELECTRICAL SPECIFICATIONS		
over the Operating Temperature Range, Supply Voltage Change, Ouput Load Change, First Year Aging at 25°C, Shock, and Vibration)Supply Voltage3.3Vdc ±10%Input Current5mA MaximumOutput Voltage Logic High (Voh)90% of Vdd MinimumInput Current Logic High (Ioh)-1.6mAOutput Voltage Logic Low (Vol)10% of Vdd MaximumInput Current Logic Low (Iol)+1.6mARise/Fall Time4nSec Maximum (Measured at 20% to 80% of waveform)Duty Cycle50 ±5(%) (Measured at 50% of waveform)Load Drive Capability15pF MaximumOutput Logic TypeCMOSLogic Control / Additional OutputTri-State (High Impedance)Tri-State Input Voltage (Vih and Vil)90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)Standby Current10µA Maximum (Disabled Output: High Impedance)One Sigma Clock Period Jitter25pSec MaximumStart Up Time10mSec Maximum	Nominal Frequency	32.768MHz	
Input Current       5mA Maximum         Output Voltage Logic High (Voh)       90% of Vdd Minimum         Input Current Logic High (Ioh)       -1.6mA         Output Voltage Logic Low (Vol)       10% of Vdd Maximum         Input Current Logic Low (Iol)       +1.6mA         Rise/Fall Time       4nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10µA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Frequency Tolerance/Stability	over the Operating Temperature Range, Supply Voltage Change, Ouput Load Change, First Year Aging at	
Output Voltage Logic High (Voh) 90% of Vdd Minimum  Input Current Logic High (Ioh) -1.6mA  Output Voltage Logic Low (Vol) 10% of Vdd Maximum  Input Current Logic Low (Iol) +1.6mA  Rise/Fall Time 4nSec Maximum (Measured at 20% to 80% of waveform)  Duty Cycle 50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability 15pF Maximum  Output Logic Type CMOS  Logic Control / Additional Output Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)  Standby Current 10µA Maximum (Disabled Output: High Impedance)  Start Up Time 10mSec Maximum	Supply Voltage	3.3Vdc ±10%	
Input Current Logic High (Ioh)       -1.6mA         Output Voltage Logic Low (Vol)       10% of Vdd Maximum         Input Current Logic Low (Iol)       +1.6mA         Rise/Fall Time       4nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10μA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Input Current	5mA Maximum	
Output Voltage Logic Low (Vol)       10% of Vdd Maximum         Input Current Logic Low (Iol)       +1.6mA         Rise/Fall Time       4nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10µA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Output Voltage Logic High (Voh)	90% of Vdd Minimum	
Input Current Logic Low (IoI)       +1.6mA         Rise/Fall Time       4nSec Maximum (Measured at 20% to 80% of waveform)         Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10μA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Input Current Logic High (Ioh)	-1.6mA	
Rise/Fall Time 4nSec Maximum (Measured at 20% to 80% of waveform)  Duty Cycle 50 ±5(%) (Measured at 50% of waveform)  Load Drive Capability 15pF Maximum  Output Logic Type CMOS  Logic Control / Additional Output Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)  Standby Current 10µA Maximum (Disabled Output: High Impedance)  One Sigma Clock Period Jitter 25pSec Maximum  Start Up Time 10mSec Maximum	Output Voltage Logic Low (Vol)	10% of Vdd Maximum	
Duty Cycle       50 ±5(%) (Measured at 50% of waveform)         Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil) Impedance)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10μA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Input Current Logic Low (IoI)	+1.6mA	
Load Drive Capability       15pF Maximum         Output Logic Type       CMOS         Logic Control / Additional Output       Tri-State (High Impedance)         Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10μA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Rise/Fall Time	4nSec Maximum (Measured at 20% to 80% of waveform)	
Output Logic Type CMOS  Logic Control / Additional Output Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)  Standby Current 10µA Maximum (Disabled Output: High Impedance)  One Sigma Clock Period Jitter 25pSec Maximum  Start Up Time 10mSec Maximum	Duty Cycle	50 ±5(%) (Measured at 50% of waveform)	
Logic Control / Additional Output Tri-State (High Impedance)  Tri-State Input Voltage (Vih and Vil) 90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)  Standby Current 10µA Maximum (Disabled Output: High Impedance)  One Sigma Clock Period Jitter 25pSec Maximum  Start Up Time 10mSec Maximum	Load Drive Capability	15pF Maximum	
Tri-State Input Voltage (Vih and Vil)       90% of Vdd Minimum or No Connect to Enable Output, 10% of Vdd Maximum to Disable Output (High Impedance)         Standby Current       10μA Maximum (Disabled Output: High Impedance)         One Sigma Clock Period Jitter       25pSec Maximum         Start Up Time       10mSec Maximum	Output Logic Type	CMOS	
Standby Current     10μA Maximum (Disabled Output: High Impedance)       One Sigma Clock Period Jitter     25pSec Maximum       Start Up Time     10mSec Maximum	Logic Control / Additional Output	Tri-State (High Impedance)	
One Sigma Clock Period Jitter     25pSec Maximum       Start Up Time     10mSec Maximum	Tri-State Input Voltage (Vih and Vil)	, · ·	
Start Up Time 10mSec Maximum	Standby Current	10µA Maximum (Disabled Output: High Impedance)	
	One Sigma Clock Period Jitter	25pSec Maximum	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-202, Method 213, Condition C	
Resistance to Soldering Heat	MIL-STD-202, Method 210	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, Method 1010	
Vibration	MIL-STD-883, Method 2007, Condition A	



### **MECHANICAL DIMENSIONS (all dimensions in millimeters)**



PIN	CONNECTION
1	Tri-State
2	Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	ECLIPTEK
2	32.768M
3	XXYZZ XX=Ecliptek Manufacturing Code Y=Last Digit of the Year ZZ=Week of the Year

### **Suggested Solder Pad Layout**

All Dimensions in Millimeters



All Tolerances are ±0.1



#### **OUTPUT WAVEFORM & TIMING DIAGRAM**



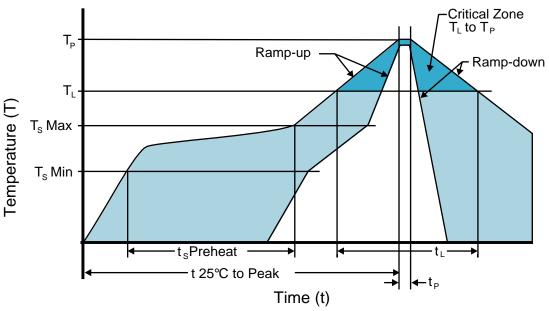
#### **Test Circuit for CMOS Output**



- Note 1: An external  $0.1\mu F$  low frequency tantalum bypass capacitor in parallel with a  $0.01\mu F$  high frequency ceramic bypass capacitor close to the package ground and  $V_{DD}$  pin is required.
- Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.
- Note 3: Capacitance value  $\dot{C}_L$  includes sum of all probe and fixture capacitance.



## **Recommended Solder Reflow Methods**



### **High Temperature Infrared/Convection**

<u> </u>	
T <sub>s</sub> MAX to T <sub>∟</sub> (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>S</sub> MIN)	150°C
- Temperature Typical (T <sub>s</sub> TYP)	175°C
- Temperature Maximum (T <sub>s</sub> MAX)	200°C
- Time (t <sub>s</sub> MIN)	60 - 180 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T <sub>P</sub> )	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T <sub>P</sub> Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.



## **Recommended Solder Reflow Methods**



### Low Temperature Infrared/Convection 240°C

T <sub>S</sub> MAX to T <sub>L</sub> (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T <sub>s</sub> MIN)	N/A
- Temperature Typical (T <sub>S</sub> TYP)	150°C
- Temperature Maximum (T <sub>s</sub> MAX)	N/A
- Time (t <sub>s</sub> MIN)	60 - 120 Seconds
Ramp-up Rate (T <sub>L</sub> to T <sub>P</sub> )	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T <sub>P</sub> )	240°C Maximum
Target Peak Temperature (T <sub>P</sub> Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1
Additional Notes	Temperatures shown are applied to body of device.

### **Low Temperature Manual Soldering**

185°C Maximum for 10 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)

### **High Temperature Manual Soldering**

260°C Maximum for 5 seconds Maximum, 2 times Maximum. (Temperatures shown are applied to body of device.)